Remarks

Applicant thanks the Examiner for the telephonic interview granted on October 10th. As discussed in the interview, claims 25-38 had been restricted as being as directed to an invention that is independent or distinct from the invention originally claimed. Applicant respectfully submitted that the restricted claims 25 and 26 were dependent on claim 16, and should not be examined as independent and distinct from claims 16-24. Therefore applicant respectfully requests that the restriction requirement of claims 25 and 26 be withdrawn. Claim 25 finds support in the specification on page 6, lines 15-19. Claim 26 is supported in the specification from page 14, line 22 to page 15, line 5.

Claim 16 has been amended by deleting "...the substrate being capable of withstanding processing over 350°C..." and instead describing the insulating substrate as a ceramic substrate selected from the group consisting of aluminum oxide, aluminum nitride, diamond, beryllium oxide, boron nitride, cordierite, mullite, silicon carbide, silicon nitride and glass ceramics. Support for this amendment may be found in the specification in the paragraph bridging pages 8 and 9. Claim 16 also has been amended to more distinctly point out that the deposited metal is melted on the metallic pads, and then cooled to form the metal bumps. Support for this amendment is found in thoughout the specification, in Examples 1 and 2 on page 14, lines 6-7 and 18-19 and in claim 16 as originally filed.

Claims 21 and 22 have been amended to more distinctly point out that metal is being

melted over the refractory metals pads of claim 19 to form the bumps. Support for this amendment is found in thoughout the specification, in Examples 1 and 2 and in claims 21 and 22 as originally filed.

Claims 16 and 19-22 were rejected as being anticipated by Wood et al. (US 3,663, 184). Wood et al. described solder bumps on a semiconductor die for "flip chip" bonding. These bumped semiconductor dice are produced by complicated processes in a silicon foundry. Applicant's invention as claimed is not a silicon semiconductor die with solder bumps for "flip chip" bonding to a matching support. Applicant's invention is a bumped ceramic package, which may be produced in a simple, straightforward process by thick film or thin film ceramic circuit techniques. The package may be used for semiconductor dice, as illustrated in Fig. 1, and the first paragraph on page 12 of the specification. Applicant's package is capable of connecting the semiconductor devices to a printed wiring board or higher level assembly. The connection to the higher level assembly is made by the metal bumps, the bumps being metals having melting points over 350° C and below the melting point of the metals forming the metallic pads.

Applicant respectfully submits that there is no teaching or suggestion in Woods et al. of providing a ceramic insulating substrate depositing a metal on the substrate, the metal having a melting point over 350 °C, and melting the metal so that it draws back onto metallic pads, forming metal bumps on the metallic pads. As has been previously mentioned, Wood et al. teach away from bumps melting above 625°F (329°C), col. 2, lines 11-12.

Claims 17-18 were rejected over Wood et al., U.S. 3,663,184 in view of Yamaji et al. (U.S. 6,159,837). Wood et al. has been discussed above. Yamaji et al. form protrusions on a semiconductor device by screen printing a curable organic coating over the semiconductor device. The organic coating has openings to the electrode pads of the semiconductor device. The openings are filled with a eutectic solder paste and the solder paste is melted on the semiconductor device to form a bump. The melting point of eutectic solder is 183° C. by using eutectic solder and curable organic coatings which will outgas and degrade above 350°C, Yamaji et al. teach away from applicant's process. Applicant's manufacturing method as now claimed utilizes temperature resistant ceramic substrates and powdered metals melting above 350°C; in examples 1 and 2 the powdered metals are melted at 1100°C. The process of Yamaji et al. makes "bumped chips" and not a ceramic electronic package having solderable metal bumps as a connecting means as in Applicant's invention. It is respectfully submitted the Wood et al. combined [with Yamaji et al. does not teach or suggest Applicant's invention of making an electronic package.

Claims 23-24 were rejected over Wood et al. (U.S. 3,663,184) in view of Kondo et al. (U.S. 5656,858). Wood et al. has been discussed previously. Kondo et al. describe forming "bumped chips", solder bumps on a semiconductor chip. Kondo et al. lay down a titanium/nickel barrier layer on the semiconductor chip, and coat the barrier layer with an adhesion layer of copper. A solder bump is formed on the copper adhesion layer. On the other hand, Applicant's

invention is a ceramic electronic package for semiconductor devices, the package having metal bumps for connecting to the next level assembly. The bumps are formed of silver or gold, not solder. When the package is to be joined to the next level assembly by soldering, the silver or gold bumps are coated with a barrier metal to prevent the silver or gold bumps from dissolving in solder as is discussed in the first paragraph of page 8 in the specification. Applicant respectfully submits that Woods et al. and Kondo et al. do not disclose or suggest manufacturing an electronic package by melting silver or gold bumps on its base, the silver or gold bumps being coated with a barrier metal.

The references cited, Wood et al., Yamaji et al. and Kondo et al., all describe depositing various metals such as nickel, gold and copper over the refractory metal barrier layer. However, they do not suggest Applicant's invention of melting these metals to form metal bumps at temperatures of 350°C up to 1100°C, or higher. Wood et al., Yamaji et al. and Kondo et al. are all limited to low melting solders due to the temperature limitations of the semiconductor devices, which are their bases.

Applicant respectfully submits that subject matter of his invention is not inherent in the prior art references, vide supra. Applicant also submits that his claims, as now amended, given their broadest reasonable interpretation are novel and clearly distinct over the prior art.

Based on the foregoing, Applicant respectfully submits that amended claims 16-24 and unexamined claims 25 and 26 describe novel methods of manufacturing electronic packages,

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and respectfully requests an early allowance.

Respectfully submitted

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